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PATENT APPLICATION

ATTORNEY DOCKET NO. 200309963-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Guenther et al.

Confirmation No.: 6718

Application No.: 10/701,881

Examiner: Dru M. Parries

Filing Date: 11/05/2003

Group Art Unit: 2836

Title: INTERMEDIATE BUS POWER ARCHITECTURE

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on March 5, 2007.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

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Respectfully submitted,
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Guenther et al.	Examiner: Dru M. Parries Art Unit: 2836
Serial No.: 10/701,881	
Filed: 11/05/03	
For: **INTERMEDIATE BUS POWER ARCHITECTURE**	
Date of Final Office Action: December 15, 2006	Attorney Docket No.: 200309963-1
Date of Notice of Appeal March 5, 2007	

May 7, 2007

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is timely provided to support the Notice of Appeal filed March 5, 2007.

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Appl. No. 10/701,881
Appeal Brief dated May 7, 2007

1. Real Party in Interest:

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

2. Related Appeals and Interferences

There are no other prior and/or pending appeals, interferences, or judicial proceedings that are related to, directly affect, or that will be directly affected by or have a bearing on the Board's decision.

3. Status of Claims

Claims 1-28 are pending in the application.

Claims 1-28 stand rejected in the application.

No claims were canceled in the application.

No claims were allowed in the application.

The rejections of claims 1-28 are appealed.

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4. Status of Amendments

No Amendments were filed subsequent to the Final Office Action.

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5. Summary of Claimed Subject Matter

Independent Claim 1

Claim 1 recites a system comprising a first set of power converters configured to convert an input power level to one or more output power levels (specification page 4, lines 26-30; Figure 2 power converters 215; or page 7, lines 13-16; Figure 4, power converters 410 converting an input voltage 420 to output power levels). The system includes a second set of power converters (specification page 5, lines 1-3; Figure 2 power converters 220; or Figure 4 power converters 415). Claim 1 further recites an interleaved intermediate bus configured to supply independent and redundant input to the second set of power converters from the one or more output power levels of the first set of power converters (specification page 5, lines 6-22; Figure 2 interleaved bus 225; or Figure 4 interleaved bus 405). For example, redundant input is provided by a redundant bus that provides independent input to a redundant power converter (specification page 9, lines 10-14 [0033]). An example of an interleaved bus is described at specification page 9, lines 1-9, paragraph [0032].

Dependent Claim 5

Claim 5 depends from claim 1 and recites that the interleaved intermediate bus includes outputs from the first set of power converters being operably connected to inputs of the second set of power converters forming multiple independent buses (specification page 5, lines 6-8; e.g. Figure 3 independent buses A-E).

Dependent Claim 6

Claim 6 depends from claim 1 and recites that the interleaved intermediate bus is configured without fault protection components (specification page 6, lines 1-2; page 5, lines 6-13 and 23-30).

Independent Claim 11

Claims 11 is directed to a computer system including a power source for providing power to one or more electronic components within the computer system (specification page 12, lines 1-6). An example power source is shown in Figure 2 block 205 or Figure 3 +48V (specification, page 4, lines 12-13).

The computer system includes a first group of non-isolated converters configured to have output signals combined to generate a first power output for a first electronic component, the first group of non-isolated converters including a redundant converter. For example, see Figure 3 a first group of non-isolated converters 315 that have outputs combined to generate +3.3V output (specification page 6, lines 8-22). The system also includes a second group of non-isolated converters configured to have output signals combined to generate a second power output for a second electronic component, the second group of non-isolated converters including a redundant converter. For example, see Figure 3 a second group of non-isolated converters 315 that have outputs combined to generate a separate output, e.g. +1.5V output (specification page 6, lines 8-22).

The system further recites a set of isolated converters each configured to convert an input voltage from a power source into an output voltage (specification page 6, lines 23-27; Figure 3 isolated converters 320). An intermediate power bus architecture is configured to provide the output voltage from one or more isolated converters from the set of isolated converters as an independent input voltage to one non-isolated converter within the first group of non-isolated converters, and an independent input voltage to one non-isolated converter within the second group of non-isolated converters (specification, page 7, lines 13+ paragraphs [0027-0030], and page 9 [0032]). For example, Figure 3 shows bus architecture 305 with independent buses A-E connected to provide independent input voltage to the different groups of non-isolated converters 315.

Dependent Claim 12

Claim 12 depends from claim 11 and recites that the intermediate power bus architecture includes multiple independent buses configured to provide the output voltage from the set of isolated converters (specification page 5, lines 6-8; e.g. Figure 3 independent buses A-E).

Dependent Claim 15

Claim 15 depends from claim 13 and recites that the intermediate power bus architecture is configured without fault protection components (specification page 6, lines 1-2; page 5, lines 6-13 and 23-30).

Independent Claim 17

Claim 17 is directed to a method of converting power (e.g. Figure 5) that comprises providing a input power and converting the input power to multiple intermediate power levels (specification page 10, lines 12-14; Figure 5 block 505 and block 510). Claim 17 recites that the multiple intermediate power levels are inputted as independent input signals to a first set of power converters including a redundant input signal (specification page 10, lines 22-24, Figure 5, block 515). The multiple intermediate power levels are interleaved to provide independent input signals to a second set of power converters including a redundant input signal (specification page 10, lines 25-31, Figure 5, block 520; or page 9 paragraphs [0032-0033]).

Dependent Claim 20

Claim 20 depends from claim 17 and recites that the interleaving provides the independent input signals without including fault protection components (specification page 6, lines 1-2; page 5, lines 6-13 and 23-30).

Independent Claim 21

Claim 21 is directed to a method of manufacturing a power conversion circuit (e.g. Figure 6 and specification page 11, lines 3-7). The method comprises positioning a plurality of power converters to convert an input voltage to a plurality of intermediate voltages (specification page 11, lines 8-10; Figure 6, block 605). At least a first group of power converters are grouped to generate a first output voltage including at least one redundant converter, and a second group of power converters are grouped to generate a second output voltage including at least one redundant power converter (specification page 11, lines 11-14; Figure 6, blocks 610 and 615).

The method further recites that outputs of the plurality of power converters are operably connected to inputs of the first group of power converters as independent intermediate buses without including fault protection components (specification page 11, lines 8-10; Figure 6, block 620). Without fault protection is explained at specification page 11, lines 19-28 and page 5 paragraph [0021]. Selected buses of the independent intermediate buses are operably connected to separate inputs of the second group of power converters without including fault protection components (specification page 11, lines 16-18; Figure 6, block 625). Without fault protection is explained at specification page 11, lines 19-28 and page 5 paragraph [0021].

Dependent Claim 22

Claim 22 depends from claim 21 and further recites that the operably connecting includes connecting each of the independent intermediate buses as a one-to-one relationship with each power converter in the first group of power converters, and as a one-to-one relationship with each power converter in the second group of power converters (specification page 8, lines 1-11; e.g. see Figure 3 multiple buses A-E).

Independent Claim 24

Claim 24 is directed to a power converting system that comprises a first power converter means for converting an input power level to an intermediate power level. One structure corresponding to the claimed function of converting is a group of isolated converters 320 that convert an input voltage to an intermediate voltage level (specification page 6, lines 23-28). Claim 24 further recites a second power converter means for converting the intermediate power level to one or more output power levels. One structure corresponding to the claimed function of converting is a group of non-isolated converters 305 that convert the voltages from the isolated converters 310 to one of more output voltages (specification page 7, lines 3-11).

Claim 24 also recites a bus means for redundantly connecting the first power converter means to the second power converter means. One structure corresponding to the function of redundantly connecting includes bus architecture 305 shown in Figure 3 (e.g. independent buses A-E) and specification page 7, lines 13-15, or bus architecture 405 shown in Figure 4. Redundancy is provided by having N+1 non-isolated converters in a group (spec. page 7, lines 23-25) and a redundant bus connected thereto (spec. page 8, lines 13-15). The bus means provides a function of supplying the intermediate power level as interleaved independent input signals to the second power converter means. A corresponding structure is the bus architecture 305 or 405 with multiple independent buses (specification page 7, lines 6-8; e.g. Figure 3 multiple independent buses A-E). An example of interleaving is described on specification page 9, lines 1-9 where independent buses A-C are interleaved to provide independent input.

Dependent Claim 26

Claim 26 depends from claim 24 and recites that the bus means is configured without fault protection components. This is explained at specification page 6, lines 1-2; page 5, lines 6-13 and 23-30. By interleaving multiple independent buses as claimed, automatic fault protection is built into the bus architecture. Thus, a consequence of the claimed system is that separate fault protection components are not required.

Dependent Claim 28

Claim 28 depend from claim 27 and recites that each group includes at least two power converters from the second power converter means, and the first power converter means is configured to generate a plurality of intermediate power levels, where each intermediate power level provides input power to no more that one converter per group from the second power converter means. For example, Figure 3 shows isolated converters 320 that generate a plurality of intermediate power levels that are outputted to independent buses A-E. The intermediate power levels (power carried by the independent buses A-E) provide input power to no more on converter per group (specification page 10, lines 29-31 and Figure 3). For example as seen in Figure 3, there are 3 groups of non-isolated converters 315 that are combined to form an output: first group of 5 converters form +3.3V, second group of 2 converters form +1.5V, and third group of 3 converters form +5V. Within a group, no two converters receive input from the same bus.

6. Grounds of Rejection to be Reviewed on Appeal

I. Whether Claims 1, 3-4, 7, 11, 17, 24-25, and 27 are unpatentable under 35 U.S.C. §102(e) as being anticipated by Figure 1 of the present application.

II. Whether Claims 5, 6, 12-15, 20-23, 26, and 28 are unpatentable under 35 U.S.C. §103(a) as being obvious over Figure 1 of the present application.

III. Whether Claims 2 and 16 are unpatentable under 35 U.S.C. §103(a) as being obvious over Figure 1 of the present application as applied to claims 1, 11, and 13 above, and further in view of De Rooij et al. (2004/0125618).

IV. Whether Claims 8-10, 18 and 19 are unpatentable under 35 U.S.C. 103(a) as being obvious over Figure 1 of the present application as applied to claims 1 and 17 above, and further in view of Barnsdale, Jr. et al. (4,685,056).

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7. Argument

I. Whether Claims 1, 3-4, 7, 11, 17, 24-25, and 27 are unpatentable under 35 U.S.C. §102(e) as being anticipated by Figure 1 of the present application.

Independent Claims 1, 17 and 24

Independent claim 1, as well as all other independent claims, stand rejected as being anticipated by Figure 1 of the present application. Pages of the Final Rejection (dated 12/15/2006) are referred to herein as "FR__." Appellant respectfully submits that Figure 1 has been misinterpreted and misunderstood, and fails to establish a prima facie anticipation rejection. For purposes of appeal, independent claims 1, 17 and 24 will be argued as a group with claim 1 as the selected claim for discussion.

The Examiner's position begins by stating that the claim term "interleaved" in regards to a bus is vague and cites Webster's dictionary for a meaning of "to arrange in alternate layers." (FR2, first paragraph). With this meaning, the Examiner's rationale for reading Figure 1 onto the claimed interleaved intermediate bus of claim 1 is phrased as an assumption:

> "One could say there are three layers of the bus in Fig. 1, each layer for each of the three different output voltages from the second converters." (FR2, lines 12-14)

This statement demonstrates a number of critical errors in the Examiner's reasoning that show the impropriety of the rejection and the misunderstanding of the circuit of Figure 1. The first error, the statement purely creates a hypothetical interpretation of Figure 1 in order to support the rejection. Nothing in Figure 1 or the corresponding text of the specification discuss layers of a bus. Figure 1 shows a common intermediate bus 100 connected to each output from all the isolated converters 105 to form a single common voltage on the bus 100 (specification page 1, lines 11-15). Figure 1 illustrates a single bus line representing the bus 100. The single common bus 100 is connected to each input of all the non-isolated

converters 110, thus supplying the same common voltage as input to every converter 110. Not even a hint of layers is found.

The different output voltages referred to by the Examiner (e.g. Figure 1: +3.3V, +1.5V, and +5V) are created by the output configuration of the converters 110. The outputs are not due to alleged different layers of the bus 100. The common bus 100 supplies the same input voltage to all the converters 110 and thus one skilled in the art would find no teaching or suggestion of different bus layers. The Examiner's assumption and interpretation of Figure 1 is not supported by the disclosure of Figure 1 even when using a broad definition from a dictionary. Thus, the reasoning of the rejection is without merit and fails to establish a prima facie anticipation rejection. The claimed element of an interleaved intermediate bus is not taught. Therefore, the rejection cannot be sustained. Since the same reasoning was applied to the rejections of all claims, all rejections are improper and should be reversed for this reason alone.

The second error is that for a 35 U.S.C. §102 reference to anticipate a claim, the reference must teach each and every element of the claim, either expressly or inherently (MPEP 2133). With regard to the claim language of "an interleaved intermediate bus configured to supply independent and redundant input to the second set of power converters," the Final Office Action states:

> "...the Examiner believes Fig. 1 reads on this because each second converter (110 of Fig.1) receives one (independent) input into it, and the input is redundant because each converter is getting the same input value." (FR2, first paragraph).

This statement contradicts itself. If each converter receives "the same input value," then the input value cannot be independent. As explained, the common bus of Figure 1 supplies a common voltage to all converters 110. If the voltage on the bus changes, then all input values to the converters 110 would change. The inputs are thus dependent, not independent. Accordingly, Figure 1 fails to teach each and every element of claim 1 and fails to establish a prima facie anticipation rejection. The rejection should be reversed.

Appellant additionally comments on the Examiner's position that the term "interleaved" in regards to a bus is vague (FR2, first paragraph). An applicant is, of course, entitled to be his or her own lexicographer (MPEP 2111.01 (IV)), and the specification and drawings make the meaning of an interleaved bus apparent in compliance with MPEP 2173.05(a) section I, which states:

> The meaning of every term used in a claim should be apparent from the prior art or from the specification and drawings at the time the application is filed. Applicants need not confine themselves to the terminology used in the prior art, but are required to make clear and precise the terms that are used to define the invention whereby the metes and bounds of the claimed invention can be ascertained. During patent examination, the pending claims must be given the broadest reasonable interpretation consistent with the specification. In re Morris, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997); In re Prater, 415 F.2d 1393, 162 USPQ 541 (CCPA 1969). See also MPEP § 2111 - § 2111.01. When the specification states the meaning that a term in the claim is intended to have, the claim is examined using that meaning, in order to achieve a complete exploration of the applicant's invention and its relation to the prior art. In re Zletz, 893 F.2d 319, 13 USPQ2d 1320 (Fed. Cir. 1989).

The meaning of "interleaved intermediate bus" is apparent from the specification and the drawings such that the metes and bounds of the claims can be ascertained. For example, the specification describes the interleaved intermediate bus as "multiple independent intermediate buses" and as "separated independent buses" where a fault on one independent bus does not affect the other independent buses (specification, page 5, lines 6-11). The specification, with reference to Figure 3, further describes an intermediate bus architecture 305 as, "configured to be interleaved to supply independent and redundant input" (specification page 7, lines 13-14, [0027]). Paragraph [0027] goes on the explain that the intermediate bus architecture includes "multiple intermediate buses (e.g. buses A-E) where each bus carries an output signal that is separate and independent from the other bus signals, making each bus A-E isolated from each other." (specification, page 7, lines 16-19). Looking at the example circuit connections of Figure 3, it discloses separate buses A-E that are not connected to each other and thus do not share or carry a common signal. Page 9,

paragraph [0032] of the specification also provides an example description of an interleaved bus. Paragraph [0033] provides an example of redundant input.

Therefore, the meaning of an interleaved intermediate bus is apparent from the specification and figures, which describe an interleaved bus as formed of independent buses that supply independent and redundant input. It is further apparent that "independent" refers to separate signals, rather than a common bus signal dependent and connected to all other signals. This meaning is consistent with the ordinary meaning of independent (e.g. Webster's dictionary: not dependent, not subject to control by others).

Conversely, Figure 1 discloses a common intermediate bus 100 that is connected to each of the output lines from isolated converters 105. Thus only a single bus is disclosed that carries the same common voltage (specification, page 1, lines 14-15). Bus 100 is not an interleaved bus as claimed. Furthermore since the common bus 100 is connected to the output from every isolated converter 105, the common voltage carried by the bus 100 is formed by and is dependent on the combination of all the signals from every isolated converter 105. The common bus 100 then supplies the common voltage to every non-isolated converter 110 as input. Thus each supplied input is not independent input but rather is dependent input since it is subject to control of the same common voltage carried on the common bus 100 and is dependent on any changes in any output single from any of the isolated converters 105. Accordingly, the Examiner's interpretation of Figure 1 is incorrect and Figure 1 fails to support a proper anticipation rejection.

In sum, claim 1 recites a system including an interleaved intermediate bus configured to supply independent and redundant input to a second set of power converters from one or more power levels of a first set of power converters. It has been shown that Figure 1 fails to teach each and every limitation of claim 1 and thus Figure 1 fails to establish a prima facie anticipation rejection. The rejection should be reversed. Accordingly, the rejections of dependent claims 2-10 are also improper and should be reversed. The claims should now be

allowed. Since independent claims 17 and 24 are grouped with claim 1, the rejections of independent claims 17 and 24, along with their dependent claims, should also be reversed.

Appellant comments on the Examiner's use of Webster's dictionary to define "interleaved" as referring to "layers." The Federal Circuit has concluded that intrinsic evidence, such as the claims, specification, and prosecution history, is the most reliable evidence by which a court can construe claim terms, whereas extrinsic evidence, including dictionaries, is less reliable and should be used for limited purposes. Phillips v. AWH Corp., 415 F.3d 1303, 75 USPQ2d 1321, (Fed. Cir. 2005) (en banc). With that in mind, the present specification does not disavow the dictionary definition from its claim scope since having layers can refer to having separate components (e.g. a three layer cake has three separate cake components). However, there is no requirement in the present claims that the multiple buses of the interleaved bus are physically stacked in layers. Although this can be one implementation, the claims are not limited to such an implementation.

Independent Claim 11

Claim 11 recites an intermediate power bus architecture configured to provide an output voltage from one or more isolated converters from a set of isolated converters as an independent input voltage to one non-isolated converter within a first group of non-isolated converters and an independent input voltage to one non-isolated converter within the second group of non-isolated converters. Claim 11 was rejected as being anticipated by Figure 1 of the present specification but the specific limitations of claim 11 were not addressed in the Final Office Action. Rather, claim 11 was summarily rejected under claim 1 (FR2) and with a conclusory rejection on page 3 (FR3). For this reason, a prima facie anticipation rejection has not been established and the rejection should be reversed.

Furthermore, Figure 1 fails to teach each feature of the claimed intermediate power bus architecture in combination with the other claimed components. Thus a proper §102 rejection has not established by Figure 1. For example, Figure 1 discloses a common

intermediate bus 100 that supplies a common voltage created from all the isolated converters 105 (see specification page 1, paragraph [0001]). Every non-isolated converter 110 is connected to the intermediate bus 100 and receives the same common voltage from the intermediate bus 100. No matter how the non-isolated converters 110 are grouped, each non-isolated converter 110 would receive the same common voltage from the single bus 100 as input, and the input is dependent on all of the outputs from the isolated converters 105.

Thus the system of Figure 1 does not disclose the claimed intermediate power bus architecture that provides an independent input voltage to one non-isolated converter within the first group of non-isolated converters and an independent input voltage to one non-isolated converter within the second group, where the groups are defined by how they generate a power output as recited in the claim. Figure 1 is a different type of bus architecture that fails to teach the claimed architecture and thus fails to establish a prima facie anticipation rejection. The rejection should be reversed. Accordingly, the rejections of dependent claims 12-16 are also improper and should be reversed.

II. Whether Claims 5, 6, 12-15, 20-23, 26, and 28 are unpatentable under 35 U.S.C. §103(a) as being obvious over Figure 1 of the present application.

Dependent Claims 5 and 12 - Multiple Independent Buses

Claim 5 depends from claim 1 and claim 12 depends from independent claim 11. claims 5 and 12 recite that the interleaved intermediate bus includes multiple independent buses. The Final Office Action states that this limitation is not taught by Figure 1 but "it would have been obvious to one of ordinary skill in the art at the time of the invention to form the intermediate bus into multiple independent buses...since it has been held that rearranging parts in an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70." (FR4, lines 6-13).

The Examiner's reliance Japikse is misplaced and does not apply to the present facts. Japikse involved moving the position of a starting switch in a hydraulic press. The court found that shifting the position of the starting switch would not have modified the operation of the device and held the claims unpatentable (see MPEP 2144.04 section VI (C)). Contrary to the facts in Japikse, the present claimed system includes a different bus structure of multiple independent buses, not merely moving the single common bus 100 of Figure 1 to a new position. Furthermore, the claimed multiple independent buses of the interleaved bus modifies the operation of the system as compared to the system of Figure 1. The claimed system provides for independent input, which Figure 1 does not provide. Also as a result of the novel bus configuration, the multiple independent buses provide for fault protection without additional fault protection components, which the common bus 100 of Figure 1 does not provide. Instead, the bus of Figure 1 includes additional fault protection components 115, 120, and 125.

Therefore, the present claims do not involve a mere rearranging of parts and Japikse does not apply. As such, Japikse fails to establish a prima facie obviousness rejection. The rejections should be reversed.

Furthermore, MPEP 2144.04(VI)(C) provides:

> However "the mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claim on appeal is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351,353 (Bd.Pat.App. & Inter. 1984). (Emphasis added).

Figure 1 is illustrates to a common intermediate bus **100** and provides no motivation or reason to make the changes proposed by the Final Rejection. The only motivation comes from the present specification. Indeed, the motivation stated in the rejection is taken from the present specification (compare FR2 with specification page 9, paragraph [0034] and page

12, paragraph [0043]). Therefore, no motivation from the prior art has been provided to suggest forming multiple independent buses between power converters as claimed. A prima facie obviousness rejection has not been established and the rejections cannot be sustained.

Dependent claims 6, 15, 20 and 26 - Bus Without Fault Protection Components

In general, each of these claims recite that the interleaved bus is configured without fault protection components. The Final Rejection states that "omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art" (FR4). The rejection relies on In re Karlson, 311 F.2d 581, 584, 136 USPQ 184, 186 (CCPA 1963). Appellant notes that the courts have also recognized that Karlson is not a mechanical rule, and that the language in Karlson was not intended to short circuit the determination of obviousness mandated by 35 U.S.C. § 103. In re Wright, 343 F.2d 761, 769-70, 145 USPQ 182, 190 (CCPA 1965).

Furthermore the Examiner's reliance on Karlson, id., is misplaced with regard to the present factual situation. Contrary to the facts presented in Karlson in which certain elements and their functions are removed and the retained elements perform the same functions as before, functions of fault protection in Appellant's claimed system are retained. In other words, Appellant's claimed system is reconfigured to perform the functions of the removed fault protection components by providing for fault protection with the interleaving of the bus (claims 6, 15, 20) that forms multiple independent buses (claim 5, 12). Providing fault protection without dedicated fault protection components is a result of the claimed interleaved bus configuration (see specification page 5, paragraphs [0019-0021]). It has been held that the omission of an element and the retention of its function is an indicia of unobviousness. In re Edge, 359 F.2d 896, 899, 149 USPQ 556, 557 (CCPA 1966).

Therefore, the Examiner's position is not supported by Karlson and in fact contradicts the authority in Edge. Thus, a prima facie obviousness rejection has not been established for claims 6, 15, 20 and 26. The rejection of these claims should be reversed.

Independent Claim 21

Claim 21 is directed to a method of manufacturing a power conversion circuit and recites operably connecting outputs of a plurality of power converters to inputs of a first group of power converters as independent intermediate buses without including fault protection components and operably connecting selected buses of the independent intermediate buses to separate inputs of the second group of power converters without including fault protection components.

The Examiner admits that Figure 1 fails to teach an intermediate bus configured without fault protection components (FR4, lines 1-2) and admits that Figure 1 fails to teach independent buses (FR4, line 6-7). To cure these deficiencies, claim 21 was rejected using the same "rearranging of parts" rationale of Japikse and the same "omission of element" rationale of Karlson as applied previously (see FR2 and FR4). It has been shown that the Examiner's reliance on Japikse and Karlson is misplaced and does not apply to the present factual situation. Therefore, the deficiencies in the disclosure of Figure 1 are not cured by the misapplied case law. Figure 1 fails to teach, suggest or make obvious the features of claim 21. Thus a prima facie §103 obviousness rejection has not been established and the rejection should be reversed. Accordingly, the rejections of dependent claims 22 and 23 should also be reversed.

Dependent Claim 22

Claim 22 depends from independent claim 21 and recites that operably connecting selected buses includes connecting each of the independent intermediate buses as a one-to-one relationship with each power converter in the first group of power converters, and as a one-to-one relationship with each power converter in the second group of power converters. Claim 22 was rejected for the same reasons as claims 5 and 12 based on Japikse and the rationale of merely rearranging parts (FR4).

As explained above, the Examiner's reliance on Japikse is misplaced and does not apply to the present facts. The one-to-one relationships between the independent intermediate buses and the groups of power converters provide a different structure and different operation as compared to the common bus of Figure 1. Thus the situation in Japikse, which involved a mere rearranging of parts without changing the operation of the device, does not exist. A prima facie obviousness rejection has not been established and the rejection should be reversed.

III. Whether Claims 2 and 16 are unpatentable under 35 U.S.C. §103(a) as being obvious over Figure 1 of the present application as applied to claims 1, 11, and 13 above, and further in view of De Rooij et al. (2004/0125618).

Claim 2 depends from independent claim 1 and claim 16 depends from independent claim 11 via claim 13. It has been shown that Figure 1 of the present application fails to teach or suggest the independent claims and fails to establish a proper §102 or §103 rejection. Thus, the rejection of claims 2 and 16 based on Figure 1 is also improper and cannot be sustained regardless of the De Rooij teachings.

IV. Whether Claims 8-10 and 18-19 are unpatentable under 35 U.S.C. 103(a) as being obvious over Figure 1 of the present application as applied to claims 1 and 17 above, and further in view of Barnsdale, Jr. et al. (4,685,056).

Claims 8-10 depend from independent claim 1 and claims 18-19 depend from independent claim 17. It has been shown that Figure 1 of the present application fails to teach or suggest the independent claims and fails to establish a proper §102 or §103 rejection. Thus, the rejection of claims 8-10 and 18-19 based on Figure 1 is also improper and cannot be sustained regardless of the Barnsdale teachings.

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Conclusion

For the reasons set forth above, neither a prima facie anticipation rejection nor an obviousness rejection has not been established for any claim. All rejections have been shown to be improper. Appellant respectfully believes that all pending claims **1-28** patentably and unobviously distinguish over the references of record and that the rejections should be reversed. Appellant respectfully requests that the Board of Appeals overturn the Examiner's rejections and allow all pending claims. An early allowance of all claims is earnestly solicited.

Respectfully submitted,

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8. Claims Appendix

1. A system, comprising:

a first set of power converters configured to convert an input power level to one or more output power levels;

a second set of power converters; and

an interleaved intermediate bus configured to supply independent and redundant input to the second set of power converters from the one or more output power levels of the first set of power converters.

2. The system of claim 1, where the first set of power converters include power transformers.

3. The system of claim 1, where the first set of power converters include isolated converters.

4. The system of claim 1, where the second set of power converters include non-isolated converters.

5. The system of claim 1, where interleaved intermediate bus includes outputs from the first set of power converters being operably connected to inputs of the second set of power converters forming multiple independent buses.

6. The system of claim 1, where interleaved intermediate bus is configured without fault protection components.

7. The system of claim 1, where second set of power converters are configured in parallel, and where the second set of power converters configured to receive the redundant input.

8. The system of claim 1, where the system is embedded in a computer system and the second set of power converters are configured to output power to one or more logic devices within the computer system.

9. The system of claim 8, where the second set of power converters have outputs that are selectively combined to generate one or more selected output levels.

10. The system of claim 1, where the system is embedded in one of, computer, an image forming device, a logic device, a printed circuit board, and a circuit.

11. A computer system including a power source for providing power to one or more electronic components within the computer system, comprising:

a power source;

a first group of non-isolated converters configured to have output signals combined to generate a first power output for a first electronic component, the first group of non-isolated converters including a redundant converter;

a second group of non-isolated converters configured to have output signals combined to generate a second power output for a second electronic component, the second group of non-isolated converters including a redundant converter;

a set of isolated converters each configured to convert an input voltage from a power source into an output voltage; and

an intermediate power bus architecture configured to provide the output voltage from one or more isolated converters from the set of isolated converters as an independent input voltage to one non-isolated converter within the first group of non-isolated converters, and an independent input voltage to one non-isolated converter within the second group of non-isolated converters.

12. The computer system of claim 11 where the intermediate power bus architecture includes multiple independent buses configured to provide the output voltage from the set of isolated converters.

13. The computer system of claim 11 where the output voltage from each of the set of isolated converters are selectively operably connected to inputs of the first and second groups of non-isolated converters. by an intermediate bus.

14. The computer system of claim 13 where the intermediate power bus architecture being configured to provide a redundant output voltage from the set of isolated converters to the redundant converter from the first and second group of non-isolated converters, respectively.

15. The computer system of claim 13 where the intermediate power bus architecture being configured without fault protection components.

16. The computer system of claim 13 where the set of isolated converters, the first group of non-isolated converters, and the second group of non-isolated converters include one of, AC power transformers, and DC power transformers.

17. A method of converting power, comprising:
providing a input power;
converting the input power to multiple intermediate power levels;
inputting the multiple intermediate power levels as independent input signals to a first set of power converters including a redundant input signal; and
interleaving the multiple intermediate power levels to provide independent input signals to a second set of power converters including a redundant input signal.

18. The method of claim 17, further including outputting one or more power levels from the first and second set of power converters to one or more electronic components.

19. The method of claim 18 where the outputting includes outputting the one or more power levels as one or more different voltage levels.

20. The method of claim 17 where the interleaving provides the independent input signals without including fault protection components.

21. A method of manufacturing a power conversion circuit, comprising:

positioning a plurality of power converters to convert an input voltage to a plurality of intermediate voltages;

grouping at least a first group of power converters to generate a first output voltage including at least one redundant converter, and a second group of power converters to generate a second output voltage including at least one redundant power converter;

operably connecting outputs of the plurality of power converters to inputs of the first group of power converters as independent intermediate buses without including fault protection components; and

operably connecting selected buses of the independent intermediate buses to separate inputs of the second group of power converters without including fault protection components.

22. The method as set forth in claim 21 where the operably connecting includes connecting each of the independent intermediate buses as a one-to-one relationship with each power converter in the first group of power converters, and as a one-to-one relationship with each power converter in the second group of power converters.

23. The method as set forth in claim 22 where the operably connecting forms an interleaved power bus including the independent intermediate buses.

24. A power converting system comprising:

a first power converter means for converting an input power level to an intermediate power level;

a second power converter means for converting the intermediate power level to one or more output power levels; and

a bus means for redundantly connecting the first power converter means to the second power converter means and to supply the intermediate power level as interleaved independent input signals to the second power converter means.

25. The power converting system of claim 24 where first power converter means includes a plurality of power converters being each configured to convert the input power level to the intermediate power level.

26. The power converting system of claim 24 where the bus means being configured without fault protection components.

27. The power converting system of claim 24 where the second power converter means include a plurality of power converters being selectively combined in groups where each group being configured to generate one output power level.

28. The power converting system of claim 27 where:

each group includes at least two power converters from the second power converter means; and

the first power converter means being configured to generate a plurality of intermediate power levels, where each intermediate power level provides input power to no more that one converter per group from the second power converter means.

9. Evidence Appendix

None. There is no extrinsic evidence.

10. Related Proceedings Appendix

None. There are no related proceedings.